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Abstract

Circuit arrangement and method for protecting an integrated semiconductor circuit

What are proposed are a circuit arrangement and a method for protecting an integrated semiconductor circuit containing a protection circuit having a thyristor structure (SCR) and also a control circuit (TC; C1, R1, I1 to I3) for driving the protection circuit, which are both connected between an element (PV, LV) to be protected and a reference potential (VB), the control circuit (TC; C1, R1, I1 to I3) generating a plurality of control signals which in each case drive an active element (T1, T2) of the thyristor structure. A targeted triggering of the protection circuit in conjunction with defined switching thresholds and short turn-on times is thereby achieved. A possibility for determining the duration of the activation of the control circuit is furthermore proposed.

Figure 1b